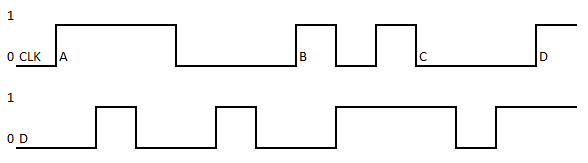
**Chapter 3 Exercise Questions**

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1. Given the input waveforms shown in the diagram, specify the output of Q at the following points of a D flip-flop (on each clock rise).(4 pts.):





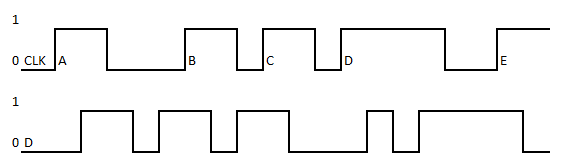
A – **0**

B – **0**

C – **1**

D – **1**

2. Given the input waveforms shown in the diagram, specify the output of Q at the following points of a D flip-flop (on each clock rise).(5 pts.):





A – **0**

B – **1**

C – **1**

D – **0**

E – **1**

3. Which of the circuits are synchronous sequential circuits? Explain (4 pts.).

**A diagram of a block diagram

Description automatically generated**

▶ Every circuit element is either a register or a combinational circuit

▶ At least one circuit element is a register

▶ All registers receive the same clock signal

▶ Every cyclic path contains at least one register.

1. **A is not a synchronous sequential circuit as there is no register(Clock),**
2. **B is not a synchronous sequential circuit as the cyclic path does not have a register, and it does not receive the same clock signal as the other circuit.**
3. **C is a synchronous sequential circuit as there is a register in the cyclic path and its synchronized by a clock signal.**
4. **D is is a synchronous sequential circuit as there is a register in the cyclic path and its synchronized by a clock signal.**

4. What is the difference between a latch and a flip-flop (3.5 pts.)? Under what circumstances is each one preferable (3.5 pts.)?

A flip-flop is Bi-stable and controlled with clocks (usually on edge triggers) where states change depending on the input, clock input and previous states. They are synchronized to the clock signals.

A latch is Bi-stable and is controlled without clocks (and has no edge triggers), making it so its states change depending only on input and previous states. Latches can only be synchronized with external signals.

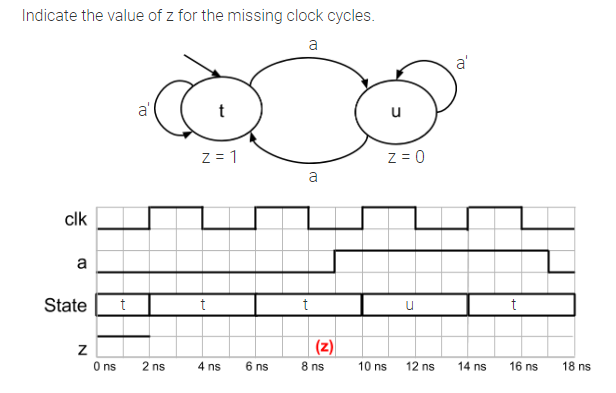
**Flip-flops are preferred if:**

* Devices need to be synchronous to clock impulses.
* Edge triggering is needed.
* You are looking for the minimum duration in clock pulses.

**Latchs are preferred if:**

* Devices are asynchronous.
* There is level sensitivity present.
* Only bi-stable memory is required or lock signal is not a necessary condition.

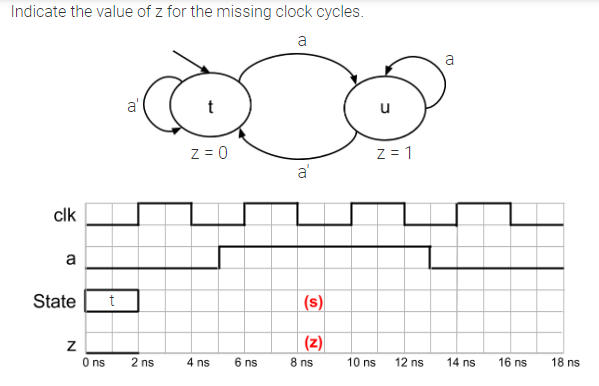
5. Indicate the value of z for the missing clock cycles at 2ns, 6ns, 10 ns and 14 ns (4 pts.).





Z – **1101**

6. Indicate the value of z and s(state) for the missing clock cycles at 2ns, 6ns, 10 ns and 14 ns (8 pts.).

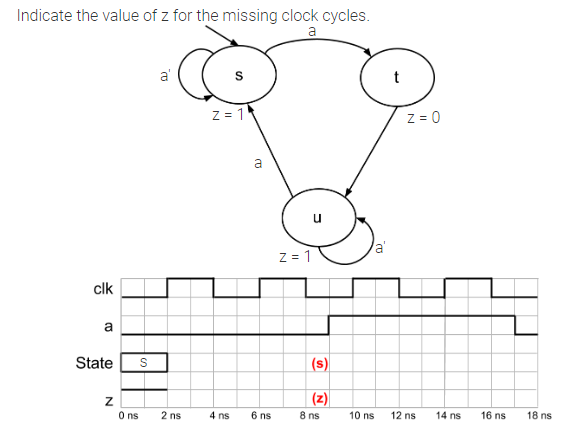




Z – **0110**

S – **TUUT**

7. Indicate the value of z and the s(state) for the missing clock cycles at 2ns, 6ns, 10 ns and 14 ns (8 pts.).





Z – **1101**

S – **SSTU**